

We Claim:

1. A test structure for a memory cell array having trench capacitors disposed in matrix form, for determining an extent of buried strap doping regions, a buried strap doping region, in a memory cell, serves as an electrode connection of an inner capacitor electrode of a trench capacitor with an associated selection transistor, the test structure comprising:

an electrical contact having a predetermined contact area and disposed between a regular matrix configuration of four of the trench capacitors, each of the trench capacitors having the inner capacitor electrode, a dielectric layer, an outer capacitor electrode isolated from the inner capacitor electrode by the dielectric layer and disposed around a lower trench region, and the buried strap diffusion region embodied as the electrode connection of the inner capacitor electrode disposed in an upper trench region.

2. The test structure according to claim 1, wherein the regular matrix configuration of four of the trench capacitors with said electrical contact disposed in between being embodied within a kerf region of the memory cell array.

3. The test structure according to claim 1, wherein the associated selection transistor has an active region disposed

below said electrical contact between the regular matrix configuration of four of the trench capacitors.

4. A memory structure, comprising:

a substrate having trenches formed therein with lower trench regions and upper trench regions;

a memory cell array having trench capacitors disposed in matrix form in said trenches, selection transistors formed in said substrate, and buried strap doping regions each serving as an electrode connection for an inner capacitor electrode and disposed in said upper trench regions, said trench capacitors having inner capacitor electrodes, dielectric layers, and outer capacitor electrodes isolated from said inner capacitor electrodes by said dielectric layers and disposed around said lower trench regions; and

electrical contacts having a predetermined contact area for determining an extent of said buried strap doping regions, each of said electrical contacts disposed between a regular matrix configuration of four of said trench capacitors for determining a short circuit between said inner capacitor electrodes and said outer capacitor electrodes.

5. The test structure according to claim 4, wherein said memory cell array has a kerf region and said regular matrix configuration with one of said electrical contacts disposed in between being embodied within said kerf region.

6. The test structure according to claim 4, wherein each of said selection transistors has an active region disposed below one of said electrical contacts between said regular matrix configuration of four of said trench capacitors.

7. The test structure according to claim 4, wherein said predetermined contact area varies in size between said electrical contacts.

8. The test structure according to claim 4, wherein said electrical contacts are each spaced differently from said trench capacitors.

9. A test structure pattern, comprising:

a plurality of test structure for a memory cell array having trench capacitors disposed in matrix form, for determining an extent of buried strap doping regions, a buried strap doping region, in a memory cell, serving as an electrode connection of an inner capacitor electrode of a trench capacitor with an

associated selection transistor, said test structures each including:

an electrical contact having a predetermined contact area and disposed between a regular matrix configuration of four of the trench capacitors, each of the trench capacitors having the inner capacitor electrode, a dielectric layer, an outer capacitor electrode isolated from the inner capacitor electrode by the dielectric layer and disposed around a lower trench region, and the buried strap diffusion region embodied as the electrode connection of the inner capacitor electrode disposed in an upper trench region; and

said electrical contact of each of said test structures having at least one of a different spacing between the trench capacitors and a different size of said contact area.